

Fig. 1A (Prior Art)

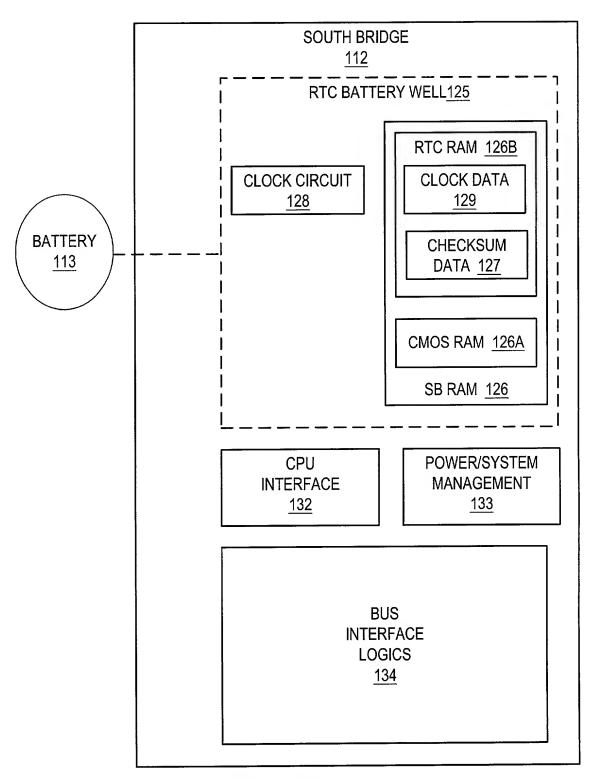


Fig. 1B (Prior Art)

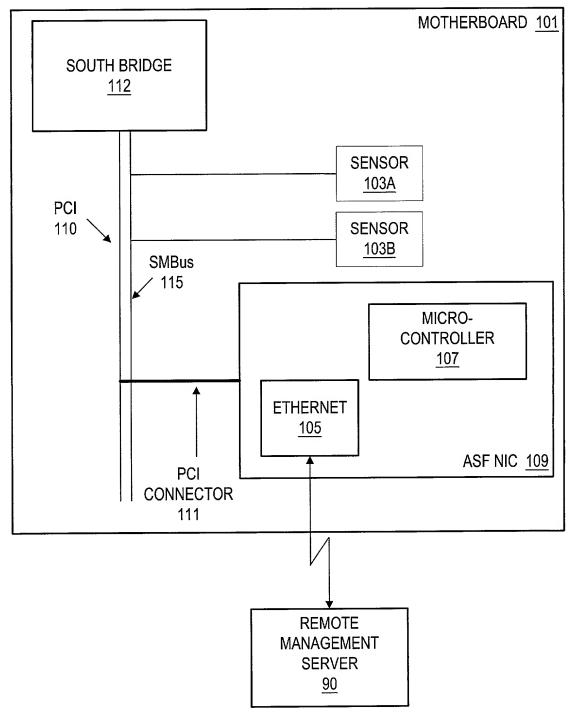


Fig. 1C (Prior Art)

135

POWER SUPPLY INITIALIZATION POWER SUPPLY GENERATES A POWER GOOD SIGNAL TO THE NORTH BRIDGE 136

UPON RECEIVING THE POWER GOOD SIGNAL, THE SOUTH BRIDGE STOPS ASSERTING THE RESET SIGNAL FOR THE PROCESSOR 138

THE PROCESSOR READS THE DEFAULT JUMP LOCATION, USUALLY AT FFFF0h 140

THE PROCESSOR JUMPS TO THE BIOS CODE LOCATION IN THE ROM BIOS, COPIES THE BIOS CODE TO RAM, AND BEGINS PROCESSING BIOS CODE INSTRUCTIONS FROM RAM 142

BIOS CODE PERFORMS POWER ON SELF TEST (POST) 144

BIOS CODE LOOKS FOR ADDITIONAL BIOS CODE, SUCH AS VIDEO @ C000h AND ATA/IDE HARD DRIVE BIOS CODE @ C800h, AND DISPLAYS A START-UP INFORMATION SCREEN 146

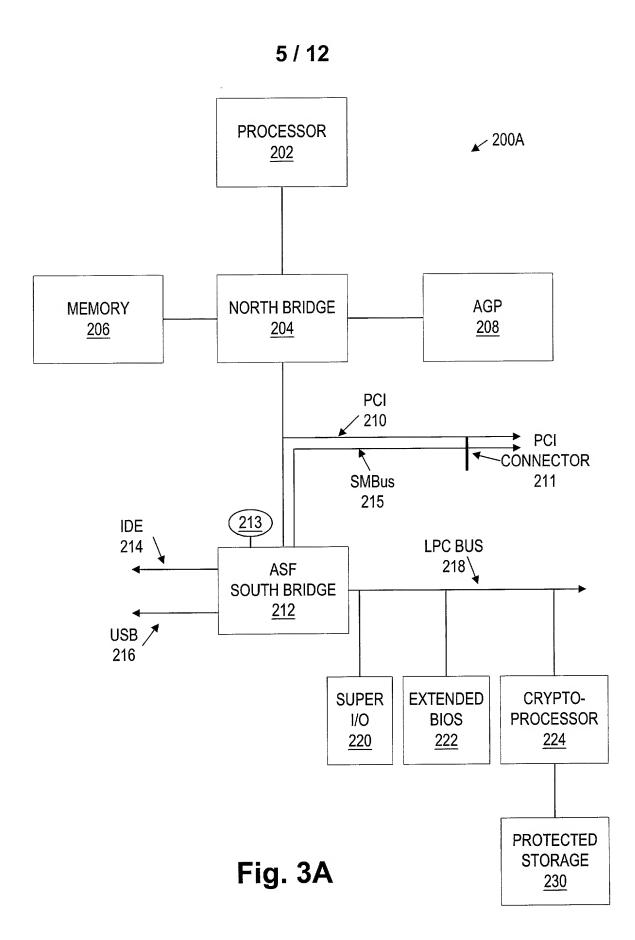
BIOS CODE PERFORMS ADDITIONAL SYSTEM TESTS, SUCH AS THE RAM COUNT-UP TEST, AND SYSTEM INVENTORY, SUCH AS IDENTIFYING COM AND LPT PORTS AND INITIALIZING THE ASF NIC 148

BIOS CODE IDENTIFIES PLUG-N-PLAY AND OTHER SIMILAR DEVICES AND DISPLAYS A SUMMARY SCREEN 150

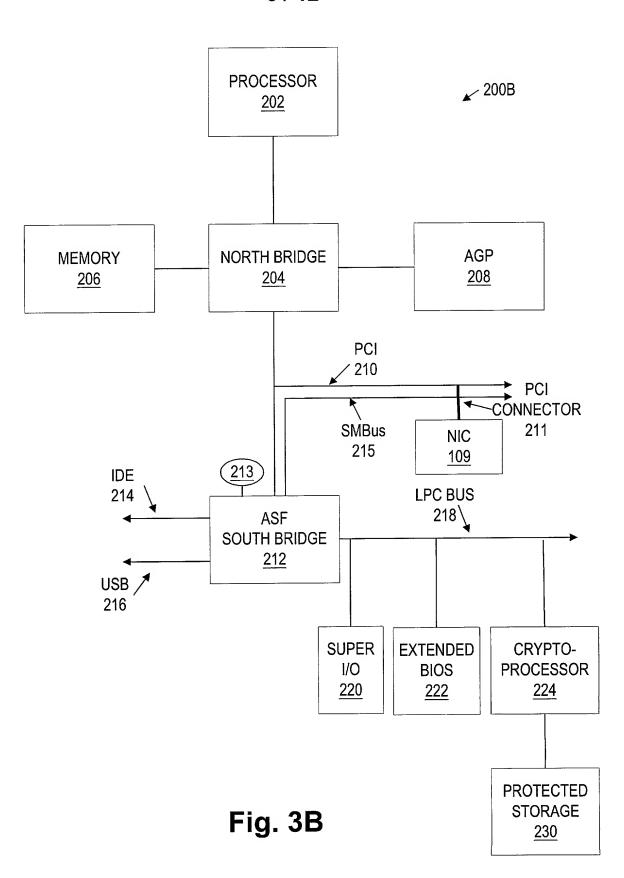
BIOS CODE IDENTIFIES THE BOOT LOCATION 152

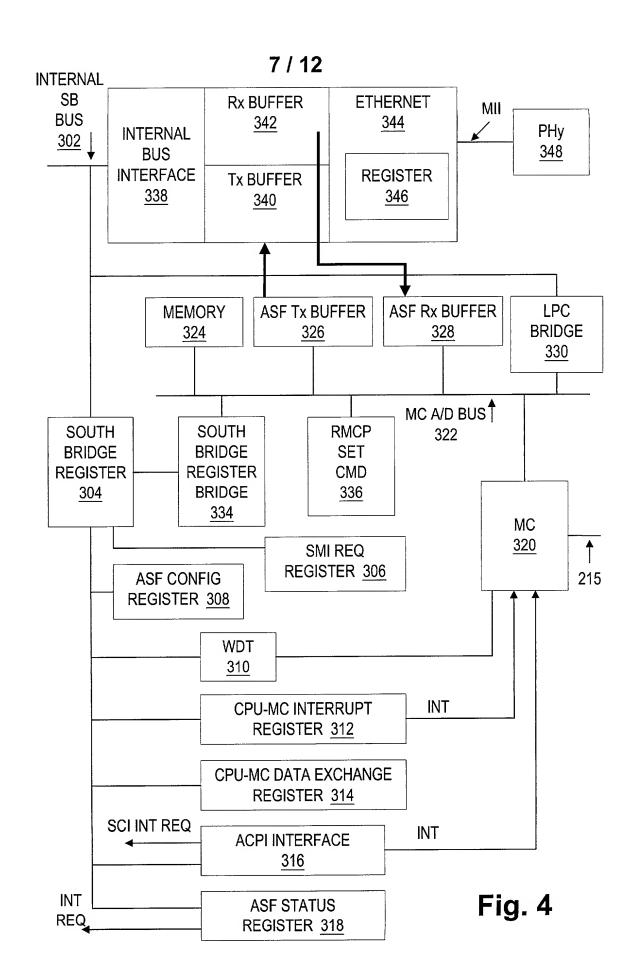
BIOS CODE CALLS THE BOOT SECTOR CODE TO BOOT THE COMPUTER SYSTEM $\underline{154}$

Fig. 2 (Prior Art)



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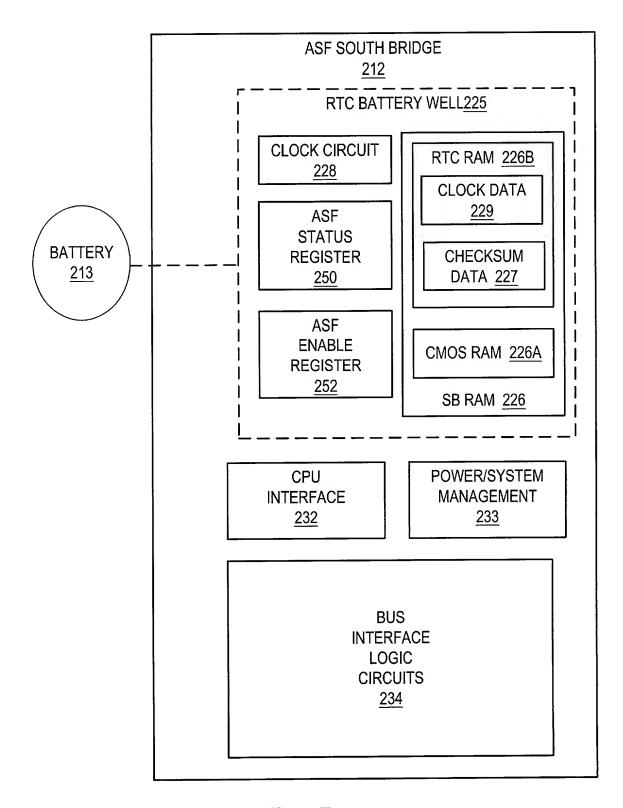


Fig. 5



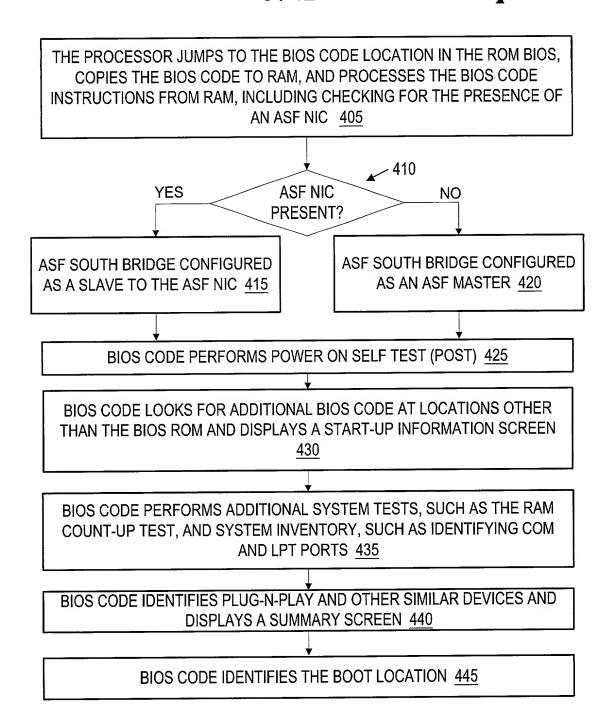


Fig. 6

500

ASF SOUTH BRIDGE IN SLAVE MODE RESPONDS TO REQUESTS FROM THE ASF NIC FOR INTERNAL SENSOR STATUS 505

ASF SOUTH BRIDGE IN SLAVE MODE RESPONDS TO SMBUS POLLS FROM THE ASF NIC 510

Fig. 7A

ASF SOUTH BRIDGE IN MASTER MODE ACTIVELY POLLS EXTERNAL SENSORS COUPLED TO THE SMBUS 605

ASF SOUTH BRIDGE IN MASTER MODE ACTIVELY POLLS INTERNAL SENSORS 610

ASF SOUTH BRIDGE IN MASTER MODE GENERATES INTERRUPTS AND RESPONDS TO INTERRUPTS 615

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Fig. 7B

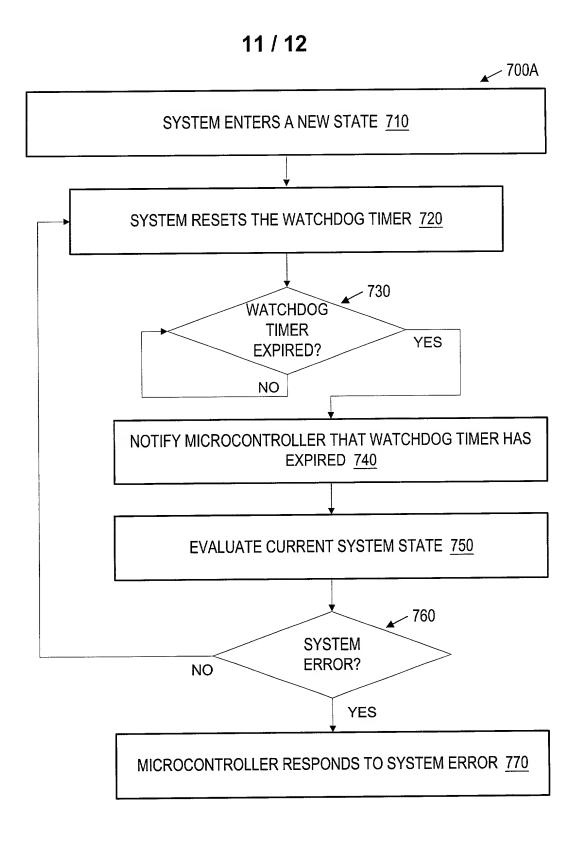


Fig. 8A

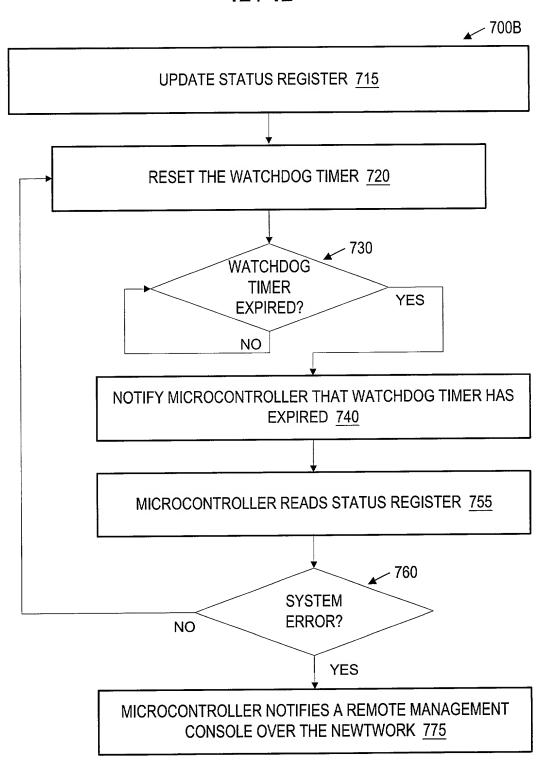


Fig. 8B